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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,852	09/25/2003	Toshiyuki Kasai	117024	4391

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,852	KASAI, TOSHIYUKI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14 and 17-28* is/are pending in the application.

4a) Of the above claim(s) *6,7,19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-5, 8-14, 17-18 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 18 September 2007 has been entered.

Election/Restrictions

2. In the response the applicant argues the restriction of claims 6-7 and 19-20, stating that independent claims 1 and 14 are generic and thus claims 6-7 and claims 19-20 should be examined. In the response, the applicant states that the examiner is narrowly reading claims 1 and 14 to Figure 3 by stating that the circuit shown in Figure 5 could be construed as being a "first circuit" when connected in series and a "second circuit" when connected in parallel. The examiner does agree that broadly reading the claims, one could make this broad interpretation, however, the applicant never responds to the examiner's argument that claim 1 and 14 require the first and second circuits to form a current mirror, and Figure 5 does not show a current mirror circuit. The applicant

provides no evidence that there are two circuits which form a current mirror if claim 5. In fact, the specification never states that there is a current mirror circuit in Figure 5, and thus if the applicant argues that Figure 5 does contain a current mirror then the applicant will be admitting that there is a 112, first paragraph problem with the specification. Thus, Figure 3 shows a current mirror and Figure 5 does not, and therefore, claims 1 and 14 are specifically drawn to Figure 3 and not Figure 5 and are not generic. The restriction was already made FINAL on the previous office action, and as demonstrated here is proper.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 4-5, 8-14, 17-18 and 21-28 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first circuit including a plurality of transistors connected in series and the second circuit unit including a plurality of transistors connected in parallel as recited in claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1 and 14 are objected to because of the following:

During the amendment which was in response to the 112, second rejection in the previous office action, the applicant has amended the claims to state: "each of the at least one of the first circuit unit and the second circuit unit having the plurality of transistors having he same driving capability". This amendment, however, still leaves

the claims indefinite because the claim is still stating "each of" while then stating "at least one of", since the applicant was trying to amend past the rejection the examiner is only objecting to the claims under the assumption that the words "each of the" were meant to be deleted from the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 14 both recite: "a switching element mutually connected to a plurality of transistors in the first circuit unit" and "at least one of the first circuit unit and the second circuit unit includes a plurality of transistors connected in series or in parallel". This renders the claims indefinite because it is unclear whether the applicant intends for the first circuit to have the plurality or whether there is an option as to whether the first or the second has the plurality. Furthermore, the claims later state: "each of the at least one of the first circuit unit and the second circuit unit having the plurality of transistors having the same driving capability", which is indefinite because it

is unclear which plurality of transistors are being referred, i.e. the plurality in the first circuit unit or the plurality connected in parallel or series.

For the purposes of examination, the examiner will assume that the first circuit has the plurality of transistors connected in series or parallel.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 4-5, 8-14, 17-18 and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 6,909,242).

Regarding claims 1, Kimura discloses an electronic circuit, comprising:

a first circuit unit (Figure 19, transistor 1907) through which a first current having a first current level passes (Figure 20A shows that current I_2 flows through transistor 1907.);

a switching element connected to a transistor in the first circuit unit (Figure 19, transistor 1905 is connected to transistor 1907);

a capacitor element (Figure 19, item 1909) to store a quantity of electric charge corresponding to the first current level (Column 6, lines 25-53 explain that electric charge stored in the capacitor is equal to I_2 at the end of the charging procedure [towards the end of the passage].);

a second circuit unit (Figure 19, transistor 1908) to generate a second current having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element (Figure 20C shows I_{EL} that flows through transistor 1908, where the current level will be different based upon the specifications of the transistors 1907 and 1908 as explain in column 6, lines 62-67.),

each of the at least one of the first circuit unit and the second circuit unit having the same driving capability (Column 6, lines 62-67 explain that the gate length and the channel width of the TFT 1907 and the TFT 1908 are equal and thus $I_{EL}=I_{data}$, which means that the transistors have the same driving capability.); and

the first circuit unit and the second circuit unit constituting a current mirror circuit through the capacitor element by turning on the switching element (Column 6, lines 18-33 and 57-58 explain that when the switching TFT is turned on, the current is supplied to the capacitor and then the current mirror circuit functions.).

Kimura does not explicitly teach that the first circuit unit of Figure 19 includes a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected.

However, Kimura does teach a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected (Figure 27B and Figure 35, see column 43, lines 27-34 and lines 38-45, and see also column 43, lines 46-50 which explain that the method of putting transistors in parallel can be applied to other circuits.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the parallel transistors taught in Figures 27B and 35 of Kimura into the first circuit of Kimura's embodiment in Figure 19 as suggested by column 43, lines 27-28 in order to have a method of further limiting possible display irregularities from developing and to average the dispersion characteristics in the TFTs (Column 43, lines 46-50).

Regarding claims 4 and 17, please refer to the rejection of claim 1.

Regarding claim 14, please refer to the rejection of claim 1, and furthermore Kimura also discloses and electronic device provided with a first signal line (Figure 19, 1902), a second signal line (Figure 19, 1901), and a plurality of unit circuits (It is inherent that the display would have a plurality of pixels shown in Figure 19.), each of the plurality of unit circuits comprising:

a switching element connected to the first signal line (Figure 19, transistor 1905), and on/off state of the switching element being controlled by switching signals supplied from the first signal line (Column 6, lines 8-12);

a first circuit unit connected to the second signal line (Figure 19 shows transistor 1907 connected to line 1901 through switching transistor 1905), a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element (Column 6, lines 18-61 explain that when the switching TFT is turned on, a current supplied from line 1901 passes through transistor 1907.); and

a capacitor and second circuit unit as described in the rejection of claim 1 (see Figure 19).

Regarding claims 8 and 21, Kimura discloses the electronic circuit and device according to claims 1 and 14.

Yumoto also discloses where the plurality of transistors being formed in a bundle (Figure 27B, where the transistors here are considered "bundled" since they are close together).

Regarding claims 9 and 22, Kimura discloses the electronic circuit and device according to claims 1 and 14.

Kimura also discloses where the first current level is higher than the second current level (Column 6, lines 62-67 explain that the gate length and channel width

determine the current characteristics and thus by optimizing these features the relationship between the currents can be made to have the claimed features.).

Regarding claims 10 and 23, Kimura discloses the electronic circuit and device according to claims 1 and 14.

Kimura also discloses where the second current level is higher than the first current level (Column 6, lines 62-67 explain that the gate length and channel width determine the current characteristics and thus by optimizing these features the relationship between the currents can be made to have the claimed features.).

Regarding claims 11 and 24, Kimura discloses the electronic circuit and device according to claims 1 and 14.

Kimura also discloses where there are electronic elements being supplied with the second current (Figure 19 shows the electronic element 1910 see also Figures 20A-20C).

Regarding claims 12 and 25, Kimura discloses the electronic circuit and device according to claims 11 and 24.

Kimura also discloses where the electronic elements is an electro-optical element or a current-driven element (Figures 20A-20C, element 1910 shown in Figure 19 is driven by the current shown.).

Regarding claims 13 and 26, Kimura discloses the electronic circuit and device according to claims 12 and 25.

Kimura fails to explicitly teach where the electronic element is an organic EL element, however, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the EL element taught by Kimura an organic EL element in order to provide for the power saving features of organic EL elements over inorganic EL elements.

Regarding claims 27 and 28, Kimura discloses an electronic apparatus having mounted therein the electronic circuit and device of claims 1 and 14 (Figure 3A).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

22 October 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER